We claim:

1. An optical transceiver module, having a serial electrical interface with an electrical output port and an electrical input port, for receiving and transmitting signals, the transceiver module comprising:

a receive path comprising:

an optical input port for receiving a first optical signal from external to the transceiver module;

a receiver eye opener for retiming and reshaping a first serial electrical data stream based on the first optical signal, the receiver eye opener having an adaptive equalizer located in the receive path; and

an electrical output port of the serial electrical interface for transmitting the retimed and reshaped first serial electrical data stream to external to the transceiver module; and

a transmit path comprising:

an electrical input port of the serial electrical interface for receiving a second serial electrical data stream from external to the transceiver module;

a transmitter eye opener for retiming and reshaping the second serial electrical data stream; and

an optical output port for transmitting a second optical signal to external to the transceiver module, the second optical signal based on the retimed and reshaped second serial electrical data stream.

2. The transceiver module of claim 1 wherein the adaptive equalizer comprises a decision feedback equalizer.

3. The transceiver module of claim 1 wherein the adaptive equalizer comprises a feedforward filter.

4. The transceiver module of claim 1 wherein the receiver eye opener further comprises a clock and data recovery (CDR) unit for recovering a clock signal from the first serial electrical data stream and coupled to transmit the clock signal to the adaptive equalizer.

5. The transceiver module of claim 4 wherein the CDR unit is located external to the receive path and recovers the clock signal from the first serial electrical data stream before retiming and reshaping.

6. The transceiver module of claim 4 wherein the CDR unit is located external to the receive path and recovers the clock signal from the retimed and reshaped first serial electrical data stream.

7. The transceiver module of claim 4 further comprising a retiming (RT) unit wherein:

the adaptive equalizer, the CDR unit and the RT unit are coupled in series in the receive path for the first serial electrical data stream; and

the CDR unit is further coupled to transmit the clock signal to the RT unit.

8. The transceiver module of claim 1 further comprising:

a coefficent module coupled to receive the first serial electrical data stream and to transmit coefficients to the adaptive equalizer.

9. The transceiver module of claim 8 wherein the coefficients are based on autocorrelation functions of the first serial electrical data stream.

10. The transceiver module of claim 8 further comprising:

at least two analog correlation modules, each for calculating an autocorrelation function of the first serial electrical data stream, wherein the coefficients are based on the calculated autocorrelation functions.

11. The transceiver module of claim 8 wherein the coefficients are transmitted as analog signals from the coefficient module to the adaptive equalizer.

12. The transceiver module of claim 1 wherein the first serial electrical data stream has a data rate of approximately 10 Gb/s or faster.

13. The transceiver module of claim 1 wherein the transceiver module comprises an XFP (10-Gigabit Small Form Factor) -compliant transceiver module.

14. The transceiver module of claim 1 wherein the retimed and reshaped first serial electrical data stream comprises an XFI (10 Gb/s serial electrical interface)-compliant electrical data stream.

15. The transceiver module of claim 1 wherein the transmitter eye opener has an adaptive equalizer located in the transmit path.

16. An optical transceiver module, having a serial electrical interface with electrical output means and electrical input means, for receiving and transmitting signals, the transceiver module comprising:

a receive path comprising:

optical input means for receiving a first optical signal from external to the transceiver module;

receiver eye opener means for retiming and reshaping a first serial electrical data stream based on the first optical signal, the receiver eye opener means having an adaptive equalizer located in the receive path; and

the electrical output means of the serial electrical interface for transmitting the retimed and reshaped first serial electrical data stream to external to the transceiver module; and

a transmit path comprising:

the electrical input means of the serial electrical interface for receiving a second serial electrical data stream from external to the transceiver module;

transmitter eye opener means for retiming and reshaping the second serial electrical data stream; and

optical output means for transmitting a second optical signal to external to the transceiver module, the second optical signal based on the retimed and reshaped second serial electrical data stream.

17. The transceiver module of claim 16 wherein receiver eye opener means further comprises means for recovering a clock signal from the first serial electrical data stream and for transmitting the clock signal to the adaptive equalizer.

18. The transceiver module of claim 16 further comprising:

means for receiving the first serial electrical data stream, calculating coefficients in response to the first serial electrical data stream, and transmitting the coefficients to the adaptive equalizer.

19. The transceiver module of claim 18 wherein the coefficients are based on autocorrelation functions of the first serial electrical data stream.

20. An integrated circuit for use in a transceiver module, the integrated circuit comprising:

a first electrical input port for receiving a first serial electrical data stream;

receiver eye opener circuitry for retiming and reshaping the first serial electrical data stream, the receiver eye opener circuitry including an adaptive equalizer; and

a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit.

21. The integrated circuit of claim 20 further comprising:

a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit;

transmitter eye opener circuitry for retiming and reshaping the second serial electrical data stream; and

a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream.

22. The integrated circuit of claim 20 wherein the adaptive equalizer comprises a decision feedback equalizer.

23. The integrated circuit of claim 20 wherein the adaptive equalizer comprises a feedforward filter.

24. The integrated circuit of claim 20 wherein the receiver eye opener further comprises clock recovery circuitry for recovering a clock signal from the first serial electrical data stream and coupled to transmit the clock signal to the adaptive equalizer.

25. The integrated circuit of claim 24 wherein the clock recovery circuitry is located external to a data path from the first electrical input port to the first electrical output port.

26. The integrated circuit of claim 24 wherein the adaptive equalizer and the clock recovery circuitry are coupled in series in a data path from the first electrical input port to the first electrical output port.

27. The integrated circuit of claim 20 further comprising:

a coefficent module coupled to receive the first serial electrical data stream and to transmit coefficients to the adaptive equalizer.

28. The integrated circuit of claim 27 wherein the coefficients are based on autocorrelation functions of the first serial electrical data stream.

29. The integrated circuit of claim 27 further comprising:

at least two analog correlation modules, each for calculating an autocorrelation function of the first serial electrical data stream, wherein the coefficients are based on the calculated autocorrelation functions.

30. The integrated circuit of claim 27 wherein the coefficients are transmitted as analog signals from the coefficient module to the adaptive equalizer.

31. The integrated circuit of claim 20 wherein the first serial electrical data stream has a data rate of approximately 10 Gb/s or faster.

32. The integrated circuit of claim 20 wherein the retimed and reshaped first serial electrical data stream comprises an XFI (10 Gb/s serial electrical interface)-compliant electrical data stream.